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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,065	11/19/2003	Douglas D. Coolbaugh	BUR920020116US1	1064
23389	7590	09/22/2005	EXAMINER	
SCULLY SCOTT MURPHY & PRESSER, PC 400 GARDEN CITY PLAZA SUITE 300 GARDEN CITY, NY 11530			GEBREMARIAM, SAMUEL A	
		ART UNIT	PAPER NUMBER	
		2811		

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/707,065	COOLBAUGH ET AL.
	Examiner Samuel A. Gebremariam	Art Unit 2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

1) Responsive to communication(s) filed on 04 August 2005.  
 2a) This action is FINAL.                            2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-20 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
 Paper No(s)/Mail Date \_\_\_\_\_.

4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_.  
 5) Notice of Informal Patent Application (PTO-152)  
 6) Other: \_\_\_\_\_.

## DETAILED ACTION

### ***Request for Continued Examination***

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/10/01 has been entered. An action on the RCE follows.

2. The amendment filed on 8/4/2005 has been entered.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 8-9, 11-12 and 14-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Chaen, US patent application No. US2002/0125575A1.

Regarding claim 1, Chaen teaches (fig. 2) a semiconductor structure comprising a high performance metal stacked inductor-having a relatively low sheet resistance (metal have low sheet resistance), the metal stacked inductor comprising at least one first layer of metal (6) which serves as an upper metal wire in the semiconductor structure (2) and a second layer of metal (10) located directly on top of the first layer of

metal (6), wherein the first layer of metal (6) and the second layer of metal are not interconnected by a via (refer to fig. 2).

Regarding claim 2, Chaen teaches (fig. 2) the entire claimed structure of claim 1 above including a third metal layer (12) located directly on top of the second layer of metal (10), wherein the second layer of metal (10) and the third layer of metal are not interconnected by a via (refer to fig. 2).

Regarding claims 3 and 4, Chaen teaches (figs 1 and 2) the entire claimed structure of claims 1 and 2 above including the metal-stacked inductor is spiral shaped (paragraph [0029]).

Regarding claim 8, Chaen teaches the entire claimed structure of claim 1 above including the first layer of metal is comprised of a low resistivity conductive material having a resistivity of about 3.0 micro-ohm\*cm or less (Chaen uses gold as the first layer of metal and gold has a resistivity of about 3.0 micro-ohm\*cm or less).

Regarding claim 9, Chaen teaches the entire claimed structure of claims 1 and 8 above the low resistivity conductive material is Au.

Regarding claims 11-12, Chaen teaches the entire claimed structure of claim 1 above including the second layer of metal is comprised of a low resistivity conductive material having a resistivity of about 3 micro-ohm\*cm or less and the second layer of metal is Au and is the same material as the first layer of metal (paragraph [0033]).

Regarding claims 14-15, Chaen teaches the entire claimed structure of claims 1 and 2 above including the third layer (12) of metal is Au having a resistivity of about 3

micro-ohm\*cm or less, the third layer of metal is the same conductive material as the first or second layers of metal ([0034]).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 5-7 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chaen in view of Park et al., US patent No. 6,395,637.

Regarding claim 5, Chaen teaches substantially the entire claimed structure of claim 1 above except explicitly stating that the first layer of metal is connected to a lower metal wiring level.

Park teaches (col. 5, lines 41-47) the first layer metal (12) is connected to lower metal wiring level.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the lower level of wiring taught by Park in the structure of Chaen in order to integrate the inductor structure with other regions of the device

Regarding claim 6, Chaen teaches (Park, col. 5, lines 41-47) the entire claimed structure of claim 1 above including the lower metal wiring level comprises a wiring region embedded within an interconnect dielectric (11).

Regarding claim 7, Chaen teaches (Park, fig. 4E) the entire claimed structure of claim 1 above including at least one wiring region (15) that lies to the periphery of the metal stacked inductor, the wherein in the at least one wiring region the second layer (15) of metal serves as a via interconnecting two metal wires (12) and (21a).

Regarding claim 19, Chaen teaches (fig. 2) a forming a first dielectric material (8) forming a first layer of metal (6) in the first dielectric material, the first layer of metal as the bottom layer of a metal stacked inductor; and forming a second layer of metal (10) on the first metal layer, wherein the first layer (6) of metal and the second layer (10) of metal are not interconnected by a via (refer to fig. 2).

Chaen does not teach providing a partial interconnect structure a lower metal wiring level located on a substrate.

Park teaches (col. 5, lines 41-47) forming active device structure such as CMOS before forming the inductor structure. Furthermore Park teaches forming contact holes (not shown) to form contact area by patterning the dielectric layer (11) and the first metal later (12). Therefore the first metal layer (12) is capable of serving as an upper metal wire of the interconnect structure and as the bottom layer of the metal stacked inductor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the lower level of wiring taught by Park in the structure of Chaen in order to integrate the inductor structure with other regions of the device

Regarding claim 20, Chaen teaches substantially the entire claimed process of claim 19 above including forming a third layer of metal (12) directly on top of the second layer of metal (10), wherein the second layer (10) of metal and the third (12) layer of metal are not interconnected by a via (refer to fig. 2).

7. Claims 10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chaen in view of Chaudhry et al. US patent No. 6,639,298.

Regarding claims 10 and 13 Chaen teaches substantially the entire claimed structure of claims 1 and 8 above except explicitly stating that the low resistivity conductive material Cu.

It is conventional and also taught by Chaudhry (fig. 9) using Cu in the process of forming a multi-layer inductor structure.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use copper in the structure of Chaen as taught by Chaudhry in order to form a high Q inductor.

8. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chaen in view of Park et al., US patent No. 6,395,637.

Regarding claim 16, Chaen teaches substantially the entire claimed structure of claims 1, 2 and 14 above except explicitly stating that the low resistivity conductive material is aluminum.

Park teaches (fig. 4C) a third metal layer (21a) that is made of aluminum.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Au in the structure of Chaen as taught by Park in order to form a high Q inductor.

Regarding claim 17, Chaen teaches substantially the entire claimed structure of claim 1 above including the first layer of metal is comprised of Cu and the second metal layer is comprised of Al (fig. 2C of Park).

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chaen, Chaudhry and in view of Park.

Regarding claim 18, Chaen teaches substantially the entire claimed structure of claim 2 above except explicitly stating that the first layer of metal is comprised of Cu, the second layer of metal is comprised of Cu and the third layer of metal is comprised of Al.

Chaudhry teaches (fig. 9) using Cu in the process of forming a multi-layer inductor structure.

Park teaches using Al as a third metal (21a) in the process of forming an inductor (fig. 4C)

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine both Cu and Al as taught by both Park and Chaudhry in the structure of Chaen in order to form a high Q inductor.

### ***Response to Arguments***

9. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection. Applicant argues that the lower-most metal layer of Chaen cannot not serve as an upper metal wiring as layer 64 of the

present invention. Chaen is silent about interconnection wirings that are beneath layer 6. However the fact that the lower metal layer is not mentioned does not mean layer 6 is not an upper metal layer. Further claim 1 of the present invention does not explicitly state the existence of lower metal wiring. Therefore the claim does not preclude layer 6 of Chaen from being read as an upper wiring layer. The examiner is to give claims their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

### ***Conclusion***

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A. Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG  
September 19, 2005

Steven Loke  
Primary Examiner

